SAT Based Rectilinear Steiner Tree Construction and its Applications in Global Routing

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Abstract

In modern large-scale circuit design, a VLSI chip may contain billions of transistors and millions of nets. In addition, there may be several hundreds of possible routes for each net. To handle the high complexity, a routing algorithm often adopts the two-stage approach, i.e. global routing followed by detailed routing. Global routing partitions the routing region into tiles without specifying the exact paths for all nets, whereas detailed routing determines the actual tracks and vias for nets.

Global routing is the basic step of routing, so this problem has received substantial attention from researchers. The goal of global routing is to determine the connection pattern for each net which is often represented by a rectilinear Steiner tree (RST). In early design stages like physical synthesis, floorplanning, interconnect planning and placement, RST can be used to estimate wireload, routing congestion and interconnect delay.

As the complexity of the circuits has increased day by day, the objective of the global router is not only limited to generating a connection pattern. Nowadays, the goal is to obtain a global routing solution that can reduce the congestion and eliminate channel overflows as well.

Additionally, modern integrated circuits often contain many obstacles such as IP cores, macro blocks, and pre-routed nets within the routing region. As a result, Obstacle-Avoiding Rectilinear Steiner Minimal Tree (OARSMT) construction emerges as a practical problem and has attracted increasing attention in the VLSI physical design community of late.

The three dimensional integrated circuit (3D IC) is an emerging area of modern VLSI design. The advantages of using 3D ICs are efficient utilization of chip area and reduction in interconnect lengths. Hence, generating an RST for interconnecting nets in 3D architectures is another big challenge in this era.

In this thesis, Pseudo-Boolean Satisfiability (PB-SAT) based solutions have been proposed for generating RSTs satisfying all the layout constraints. Experimental results obtained by applying the proposed method on ISPD 98 modified benchmarks show that the proposed algorithms can solve the RST problem effectively even though the circuits are very large and complex.